REMARKS

The present amendment is responsive to the Office Action dated February 13, 2009. Claims 1, 4, 10, 13, 25, 28, 34-36 and 38 have been amended. No new matter has been introduced by these amendments. Claims 1-39 are again presented for the Examiner's consideration in view of the following remarks. The rejections will be addressed in view of the claims as currently presented.

The Abstract and certain claims have been objected to due to several informalities. These informalities have been corrected as indicated herein. Therefore, applicant respectfully requests that these objections be withdrawn.

Turning to the rejections, the first rejection is for non-statutory obviousness-type double patenting against claims 1, 10 and 25 based upon purportedly similar claim language in counterpart application 10/849,623. A similar rejection against claim 37 was made over the '623 application in view of U.S. Patent No. 5,913,068 ("*Matoba*"). Applicant notes that the instant application was filed two months prior to the '623 application. As these rejections are merely provisional, they will be addressed upon allowance of either case.

Turning to the rejections based upon prior art, claims 1-3, 8-12, 19-22, 24-27, and 32-33 were rejected under 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 6,141,762 (*Nicol*) in view of U.S. Patent No. 6,345,362 (*Bertin*). Claims 4-7, 13-18, and 28-31 were rejected under 35 U.S.C. § 103(a) as being obvious over *Nicol* in view of *Bertin*, and further in view of U.S. Patent No. 5,913,068 (*Matoba*). Claim 23 was rejected under 35 U.S.C. § 103(a) as being obvious over *Nicol* in view of *Bertin* and further in view of U.S. Patent Publication No. 2002/0091954 (*Rhee*). Claims 34-35, and 38 were rejected under 35 U.S.C. § 103(a) as being obvious over *Nicol* in view of *Matoba*. And claims 36-37, and 39 were rejected under 35 U.S.C. § 103(a) as

being obvious over *Nicol* in view of *Matoba*, and further in view of *Bertin*. Of the claims rejected, claims 1, 10, 25 and 34 are independent. Applicant respectfully traverses the rejection.

As features of claims 1, 10 and 25 are generally related, they will be addressed first. These three independent claims pertain to monitoring processor tasks and loads of processors in a multi-processor system. Some of the tasks are reallocated so that at least one processor is not scheduled to perform a task, which permits such processors to enter a low power consumption state.

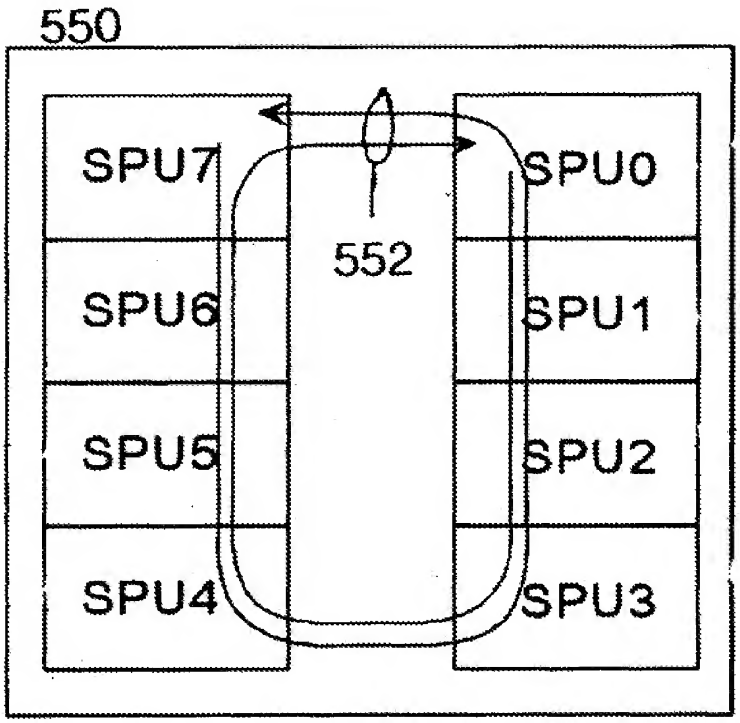
The rejection of claims 1, 10 and 25 admits that *Nicol* does not disclose at least one processor not being scheduled to perform a task and having such processor enter a low power consumption state. According to the rejection, *Bertin* "teaches a main CPU with a plurality of functional units (sub-processors) that lowers the power consumptions state to a lower or lowest level of any of the functional units that are not scheduled to be used in execution (col. 4, lines 54-61, col. 3, lines 49-54, Abstract)." (Office Action, p.12.) While *Bertin* does teach minimizing the power level of processors which do not have an instruction to execute, this is not what is claimed.

By way of example, claim 1 requires "re-allocating at least some of the tasks based on their associated processor loads such that at least one of the sub-processing units is not scheduled to perform any tasks; and commanding the sub-processing units that are not scheduled to perform any tasks into a low power consumption state."

Neither *Nicol* nor *Bertin* teaches or suggests the claimed reallocation so that a sub-processing unit does not have a task to perform. The applied combination of these references also does not provide for such a feature as claimed. In order to further clarify this, claims 1, 10 and 25 have been modified to show that the sub-processing units not scheduled to perform any tasks because of the reallocation should enter a lower power consumption state.

Turning to independent claim 34, this claim is directed to an apparatus having a particular bus configuration.

Here, the bus circularly interconnects multiple sub-processing units. Such a configuration is shown, by way of example only, in applicant's FIG. 12, which is reproduced below.



Paragraphs 0064-65 of applicant's specification discuss FIG. 12, and are reproduced below (emphasis added).

[0064] Reference is now made to FIG. 12, which is a block diagram illustrating one or more further aspects of the present invention. In this embodiment of the invention, a multi-processing system 550 includes a plurality of sub-processing units SPU0-7 that are sequentially interconnected by way of an internal bus 552. Processor task transfers from one SPU to another SPU may pass sequentially through one or more intermediately coupled SPUs unless the transfer is between adjacent SPUs. For example, a processor task migrating from SPU0 to SPU1 may simply be transferred sequentially from SPU0 to SPU1 over the internal bus 552. On the other hand, a processor task migration from SPU0 to SPU3 may pass through SPU1 and SPU2 or may pass through SPU7, SPU6, SPU5, and SPU4. **This circular structure is preferable to a bumper-to-bumper arrangement where the SPUs are sequentially interconnected in a linear (not circular) arrangement**. Indeed, with a linear arrangement there may be an excess latency in transferring processor tasks between SPUs that are disposed at extreme ends of the bus. **With the circular arrangement**

of FIG. 12, however, latencies are reduced because processor tasks may be transferred in either of two directions through the bus 552.

[0065] It is noted that the multi-processing system 550 does not include a main processing unit or PU to manage the allocation and/or migration of tasks among the SPUs. Instead, a task table (which may be substantially similar to that described hereinabove with respect to FIGS. 6-10) may be shared among the SPUs and/or may be distributed among the SPUs. In any case, the SPUs may utilize the task table 502 to migrate the processor tasks among the SPUs to achieve the power management advantages described in detail in the other embodiments of this description.

The rejection relies on *Nicol* for purportedly disclosing a circular bus; however, the reference does **not** disclose such a structure. FIG. 2 of *Nicol* and the cited portions of that reference (e.g., col.4 ll.38-53) do not teach or otherwise suggest a circular bus as claimed.

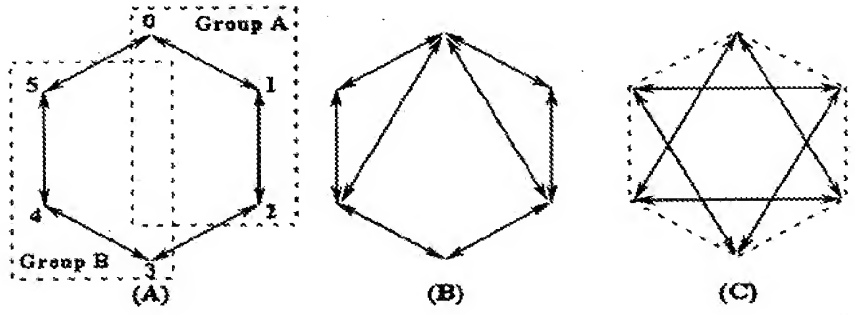
In view of the above, applicant submits that the applied combinations of references do not render independent claims 1, 10, 25 and 34 obvious. Therefore, applicant requests that the rejections of these independent claims be withdrawn.

Furthermore, claims 2-9, 11-24, 26-33 and 35-39 depend from independent claims 1, 10, 25 and 34, respectfully, and contain all the limitations thereof. For at least this reason, applicant submits that the dependent claims are likewise in condition for allowance.

Notwithstanding this, the dependent claims are separately patentable over the applied art. By way of example only, dependent claim 36 recites "wherein the re-allocation of the tasks is performed such that at least one of the sub-processing units is not scheduled to perform any tasks." As with claims 1, 10 and 25, the cited art does not teach reallocation of tasks so that at least one sub-processing unit is not scheduled to perform any tasks as claimed. Therefore, claim 36 is patentable over the cited art.

And dependent claim 35 recites "wherein the sub-processing units are arranged in groups and the re-allocation of one or more tasks of a sub-processing unit within a given one of

the groups maintains such tasks within the given group." By way of example only, an arrangement of the sub-processors into groups (e.g., as part of the circular bus configuration) is shown in FIG. 13 and is described in paragraphs 0065-66. This figure and the description from paragraph 0066 are reproduced below (emphasis added).



[0066] It is noted that even with the circular arrangement of FIG. 12, latency and other processing issues may arise in connection with transferring processor tasks between extreme ends of the structure, such as between SPU0 and SPU4. Thus, it is desirable to segregate the SPUs into two or more groups. **For example, as illustrated in FIG. 13A, SPU0, SPU1, and SPU2 may be organized into group A, while SPU3, SPU4, and SPU5 may be organized into group B. With this arrangement, processor tasks would only be transferred among the SPUs in a given group, thereby reducing latency problems and/or other barriers to efficient multi-tasking**. Further, any sharing and/or distribution of a task table may be limited to the SPUs of a given group, thereby further improving the efficiency of task processing and migration. FIGS. 13B and 13C illustrate alternative groupings and permissible task transfers between SPUs. Those skilled in the art will appreciate that many other modifications (including numbers of SPUs in the system) may be made without departing from the spirit and scope of the invention.

Applicant submits that the art of record does not disclose the claimed configuration set forth in dependent claim 35. Therefore, applicant requests that the rejection of this claim be withdrawn.

As it is believed that all of the rejections set forth in the Office Action have been fully met, favorable reconsideration and allowance are earnestly solicited.

If, however, for any reason the Examiner does not believe that such action can be taken at this time, it is respectfully requested that he telephone applicant's attorney at (908) 654-5000 in order to overcome any additional objections which he might have. If there are any additional charges in connection with this requested amendment, the Examiner is authorized to charge Deposit Account No. 12-1095 therefor.

Dated: July 13, 2009

Respectfully submitted,
Electronic signature: /Andrew T. Zidel/
Andrew T. Zidel
Registration No.: 45,256
LERNER, DAVID, LITTENBERG,
KRUMHOLZ & MENTLIK, LLP
600 South Avenue West
Westfield, New Jersey 07090
(908) 654-5000
Attorney for Applicant

1039588_1.DOC